REMARKS[1]

In the outstanding Office Action, the Examiner rejected claims 1-34 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,546,544 to Kawakami ("Kawakami") in view of U.S. Patent No. 6,225,025 to Hoshino ("Hoshino"). No claims are amended herein, and claims 1-34 remain pending in this application.

Applicants respectfully traverse the rejection of claims 1-34 under 35 U.S.C. § 103(a) because a *prima facie* case of obviousness has not been established. To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure. " *See* MPEP § 2143, 8th Ed. (Rev. 4), October, 2005. At a minimum, the Examiner has failed to establish a *prima facie* case of obviousness because the references, whether taken alone or in combination, fail to teach or suggest each and every element of the claims.

In the Office Action, the Examiner appears to assert that Kawakami teaches all of the elements in claims 1-34 except for "the use of standard cells on CP apertures listed

1 The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement of characterization in the Office Action.

in an order of frequency of use according to a difference between a VSB shot number and a CP shot number, as recited in claims 20-23, 25, 27, 29-31, and 33." Office Action, page 12. Applicants respectfully disagree with the Examiner's assertion, because Kawakami fails to teach or suggest every element in at least independent claims 1, 7, and 15. For example, Kawakami fails to teach or suggest "conducting logic synthesis for the CP apertures [and] selecting one of the CP apertures ... which has the highest throughput in delineating one of the patterns," and "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15.

Kawakami teaches:

> generating a pattern group for each layer of the integrated circuit including a plurality of the basic elements; analyzing the degree of frequency at which each basic element is used in the integrated circuit; selecting from the pattern group a pattern used as a plurality of the block patterns based on the analyzed degree of frequency at which each basic element is used... (col. 5, lines 28-35)

wherein

> by reference to the cell reference frequency information 75 and the system restraint information/mask restraints 72, the cells to be changed to masks are determined thereby to produce a mask layout A76 (col. 8, lines 17-20).

Kawakami is silent as to selecting the block pattern based on throughput, and is also silent as to analyzing the degree of frequency again to select the block pattern. Kawakami thus fails to teach or suggest "conducting logic synthesis for the CP apertures [and] selecting one of the CP apertures ... which has the highest throughput

in delineating one of the patterns," and "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the pattern," as recited in independent claims 1, 7, and 15.

The Examiner, however, asserts that based on Applicants' specification "the subject limitation refers to the steps for designing two different devices A and B, where the system constraint of designing device A using standard cells only, is subsequently removed prior to designing device B." Office Action, page 5 (emphasis added). In addition, the Examiner further asserts that Kawakami and claims 1, 7, and 15, "both perform multiple device design layouts using a stored standard cell library." Office Action, page 8. Applicants disagree with the Examiner's assertions. Here, the Examiner has not only mischaracterized claims 1, 7, and 15, but has also improperly attempted to read limitations of the specification into the claims.

The Manual of Patent Examining Procedure (MPEP) states:

> [d]uring patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification,"

and that the

> importation of subject matter from the specification into the claim [is impermissible]. MPEP § 2111, 8th Ed. (Rev. 4), October, 2005.

Accordingly, even if the Examiner were correct that Applicants' specification "refers to the steps for designing two different devices A and B, where the system constraint of designing device A using standard cells only, is subsequently removed prior to designing device B," the rejection under 35 U.S.C. § 103(a) is improper not only

because Kawakami fails to teach or suggest each and every element recited in claims 1, 7, and 15, but also for the additional reason that the Examiner has impermissibly read limitations from the specification into claims 1, 7, and 15.

Kawakami also fails to teach or suggest a combination including "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15. The Examiner concedes that Kawakami fails to teach or suggest this element, stating "neither the applicant nor Kawakami (544) constrain the design of subsequent devices to standard cell layouts previously selected for any other device design i.e., when 'conducting logic synthesis again', as recited in claims 1, 7, and 15." Office Action, page 8 (emphasis added).

Hoshino, cited by the Examiner at page 12 of the Office Action for allegedly teaching "a method of fabricating semiconductor devices with electron beam lithography that utilizes mask's having block (CP) apertures formed using shot number analysis based on frequency of use," fails to cure the above-noted deficiencies of Kawakami. Hoshino teaches:

> the exposure data verifying function 12 includes a pattern data display function 20 used for displaying a pattern data, an exposure data analysis unit 21 used for carrying out an analysis of the exposure data [created] by the exposure data creation function 11, and exposure throughput calculation function 22 for calculating the throughput of the exposure data creation function... (col. 8, lines 17-24)

wherein

> the exposure data is created in the exposure data creation function 11 such that the exposure time is minimized, by reducing the exposure data size (col. 9, lines 49-51).

Hoshino thus teaches creating exposure data in order to minimize the exposure time. This cannot constitute a teaching of "conducting logic synthesis for the CP apertures [and] selecting one of the CP apertures ... which has the highest throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15. Moreover, Hoshino is silent as to "conducting logic synthesis again," and thus fails to teach or suggest "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the pattern," as also recited in independent claims 1, 7, and 15.

Because the references fail to teach or suggest every element recited in independent claims 1, 7, and 15, a *prima facie* case of obviousness has not been established. Accordingly, Applicants request that the Examiner withdraw the rejection of claims 1, 7, and 15 under 35 U.S.C. § 103(a).

Claims 2-6, 22-26 and 34, claims 8-14 and 27-29, and claims 16-21 and 30-33 respectively depend from independent claims 1, 7, and 15, and thus require all of the respective elements of claims 1, 7, and 15. Because Kawakami in view of Hoshino fails to teach or suggest every element recited in claims 1, 7, and 15, that combination of references also fails to teach or suggest every element required by the dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims 2-6, 8-14, and 16-34 under 35 U.S.C. § 103(a).

Applicants further note that claims 1, 7, and 15 also recite that the logic synthesis is conducted "using only the standard cells ... placed ... on the ... CP apertures," and thus "convert[ing] the logic expressions into connections of standard cells," which includes the standard cells placed on the CP aperture. Therefore, it is possible to "select[] one of the CP apertures ... which has a throughput higher than a desired throughput," after logic synthesis is completed. That is, consistent with the claimed invention, the CP aperture is selected before producing the layout data, in which the standard cells are arranged, resulting in reduced semiconductor device development time.

Kawakami and Hoshino, however, both fail to describe designing the layout of the semiconductor device using standard cells placed on the CP aperture used for manufacturing the semiconductor device. Kawakami describes that mask data is produced by extracting the cells from the device's layout data, which is produced by using standard cells library and the device designing (logic synthesis). However, the device's layout data is produced regardless of the cells placed on the CP aperture, although cells to be placed on the CP aperture are selected from standard cells library. Furthermore, the cells library of the present invention also includes information of the CP aperture. Therefore, Kawakami substantially differs from independent claims 1, 7, and 15. Moreover, Kawakami includes system restraint information/mask restraints 72, as shown in FIG. 5. However, the restraint is about the layer and size of a cell, not about the device designing (col. 8, lines 25-34). Claims 1-34 are thus allowable over the cited references for this additional reason.

This Request for Reconsideration does not include any claim amendment, and thus does not raise any new issues requiring a new search. Entry of this Request for Reconsideration and a timely allowance of the pending claims is earnestly requested.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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